



BRAD DEVICES

Built in Africa, for the World

BradXon Platform Specification

Gen 1 Flagship System-on-Chip Architecture

Revision 1.0 — Gen 1 — July 2026

Target: SF4X (4nm-class), 125–750 W, 32+ cores, 1 TB/s+ fabric

Tape-out target: H1 2027

Confidential — Brad Devices Proprietary

Contents

1	Introduction	3
1.1	Platform Position	3
1.2	Key Design Goals	3
2	Adaptive Neural Fabric (ANF)	3
2.1	What ANF is not	3
2.1.1	Gen 2 Vision	4
3	BradXon Memory Map	5
3.1	System Address Map (32-bit physical)	5
3.2	64-bit Extension	6
4	Platform IP Blocks	7
4.1	XIC — BradXon Interrupt Controller	7
4.2	System Timer	7
4.3	UART — Debug Console	7
4.4	GPIO — General-Purpose I/O	8
4.5	WDT — Watchdog Timer	8
4.6	DMA — Direct Memory Access Controller	8
4.7	I2C Controller	8
4.8	SPI Controller	9
4.9	RTC — Real-Time Clock	9
4.10	PMU — Power Management Unit	9
4.11	CRU — Clock and Reset Unit	10
5	Clock Architecture	11
5.1	Reset Domains	11
6	Boot Flow	12
7	Chiplet Topology	13
7.1	Package Configurations	13
7.2	Fabric Routing	13
8	Power Architecture	14
8.1	Voltage Rails	14
8.2	Power States	14
9	Peripherals and I/O	15
9.1	Integrated Peripherals	15
9.2	PCIe Root Complex	15
10	Security Architecture	16
10.1	HSM Specifications	16
11	Revision History	17

1 Introduction

BradXon is the flagship BradCore platform tier, designed for maximum compute density, bandwidth, and power envelope. It targets high-end workstations, gaming consoles, and datacentre accelerators using chiplet-based SF4X (4nm-class Samsung) silicon, the BradFusion mesh fabric, and next-generation memory interconnects.

1.1 Platform Position

Table 1: BradCore platform hierarchy

Platform	TDP Range	Process	Target
BradMind Lite–Elite	2–45 W	7LPP/SF4	Mobile, thin laptop
BradNeuro Ultra–Elite	45–125 W	SF4P/SF4X	Gaming, pro mobile
BradXon	125–750 W	SF4X (4nm)	Desktop, WS, rack

1.2 Key Design Goals

1. **Chiplet scalability:** 1–4 chiplets per package, unified cache-coherent address space via BradFusion mesh
2. **Memory bandwidth:** HBM3e (stacked) + DDR5/LPDDR6 (slot), target >1 TB/s aggregate
3. **I/O throughput:** PCIe 6.0 root complex (64 GT/s), 10+ GbE, USB4 v2, NVMe over fabric
4. **Deterministic power:** Configurable TDP from 125 W (compact workstation) to 750 W (multi-chiplet elite)
5. **Hardware security:** Dedicated HSM, memory encryption (AES-256-GCM), secure boot chain, attestation

2 Adaptive Neural Fabric (ANF)

2.1 What ANF is not

ANF does not re-form silicon at runtime. The physical execution arrays — CPU P/E cores, BradVector shader dies, Neuro-Stream NPU slices — are fabricated once and never morph into one another. What is adaptive is *how the fabric composes and budgets* those fixed arrays. Three mechanisms make the fabric adaptive:

1. **Compute Partitions (CPs).** The die’s execution arrays are grouped into hardware partitions composed at boot under secure zone isolation (MMU + L6-Xon). A partition is branded CPU-side, GPU-side, or NPU-side; partitions are created, destroyed, and re-allocated at domain boundaries — never per instruction. Partition ownership is fenced by the security engine, so a stolen partition cannot become a covert path.
2. **Reconfigurable Dataflow Array (RDA).** The NPU slice is not a fixed systolic pipe. It is a coarse-grained reconfigurable dataflow fabric (CGRA-class) whose routing and function units are programmed at kernel launch: the AI math adapts to the model, not the model to the pipe.
3. **Fabric Governor (FG).** The PMU and OS scheduler continuously steer the shared budget — clock, power, and fabric bandwidth — between the CPU/GPU/NPU partitions (DVFS + heterogeneous scheduling). Reallocation of *budget* on demand is real; reallocation of *silicon* is not.

Table 2: ANF register map (base: 0x11000000 — fabric device MMIO)

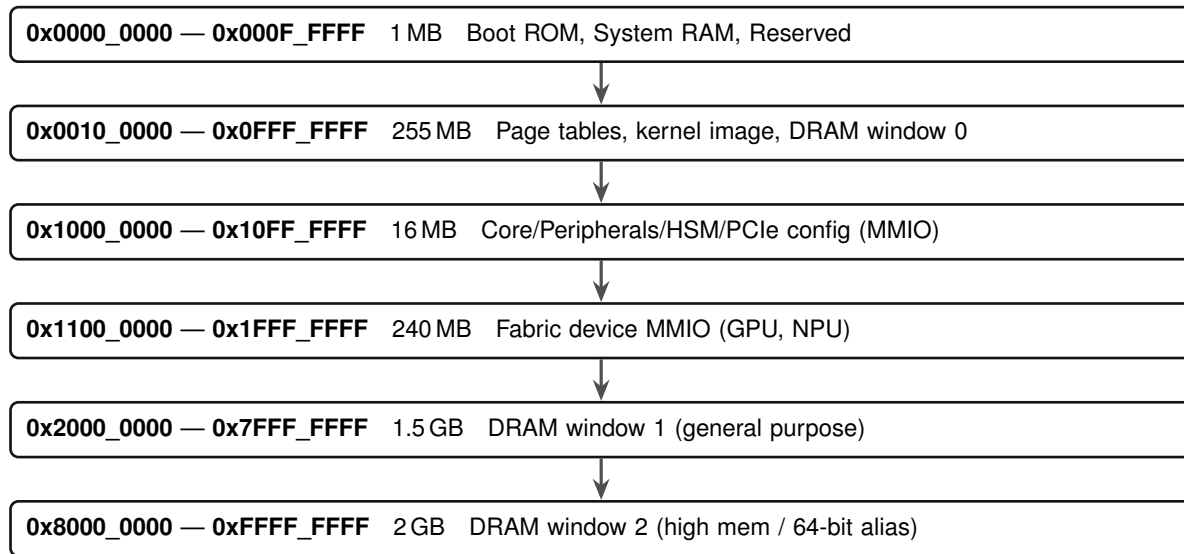
Offset	Name	Width	Description
0x0000	ANF_CTRL	32	Fabric governor enable, partition audit
0x0004	ANF_STATUS	32	Active partitions, governor state
0x0010	ANF_PT_CFG	32	Partition count, composition policy
0x0014	ANF_PT_OWNER	32	Per-partition owner domain (CPU/GPU/NPU)
0x0018	ANF_PT_SEC	32	Partition security fence / zone tag
0x0020	ANF_GOV_POLICY	32	Headroom policy: balanced / latency / batch
0x0024	ANF_GOV_EVENT	32	Budget-steering event (interrupt) mask
0x0030	ANF_RDA_BASE	32	RDA program base address (fabric-local)
0x0034	ANF_RDA_STATUS	32	RDA load/run/busy state
0x0040	ANF_FAB_QOS	32	Fabric bandwidth reservation per domain

2.1.1 Gen 2 Vision

The literal re-form — execution-unit tiles that change domain function at runtime — is Gen 2 VISION. The honest path is *tile composition at integration*: fabric tiles floorplanned as CPU, GPU, or NPU and mated into a package, composed at the factory or a field-service boundary, not per instruction. Even that is a packaging and assembly decision, not a device-physics one; it stays labelled Vision until cost and yield argue otherwise.

3 BradXon Memory Map

3.1 System Address Map (32-bit physical)



bands not to scale — see table for exact spans

Figure 1: BradXon system address layout (32-bit physical)

Table 3: BradXon physical memory map (32-bit, 4 GiB)

Base	End	Size	Region
0x00000000	0x0003FFFF	256 KB	Boot ROM (mask ROM, read-only)
0x00040000	0x0007FFFF	256 KB	System RAM (stack, heap early init)
0x00080000	0x000FFFFFFF	512 KB	Reserved
0x00100000	0x00FFFFFFF	15 MB	Page tables, kernel image (loaded by boot ROM)
0x01000000	0x0FFFFFFF	240 MB	DRAM window 0 (HBM or DDR)
0x10000000	0x1000FFFF	64 KB	Core complex MMIO (per-core control)
0x10010000	0x1001FFFF	64 KB	Interrupt controller (XIC)
0x10020000	0x1002FFFF	64 KB	System timer / counter
0x10030000	0x1003FFFF	64 KB	UART / debug console
0x10040000	0x1004FFFF	64 KB	GPIO / pinmux
0x10050000	0x1005FFFF	64 KB	Watchdog timer
0x10060000	0x1006FFFF	64 KB	DMA controller
0x10070000	0x1007FFFF	64 KB	I2C controller
0x10080000	0x1008FFFF	64 KB	SPI controller
0x10090000	0x1009FFFF	64 KB	RTC / battery-backed SRAM
0x100A0000	0x100AFFFF	64 KB	Power management unit (PMU)
0x100B0000	0x100BFFFF	64 KB	Clock / reset controller (CRU)
0x100C0000	0x100FFFFFFF	256 KB	Peripheral expansion
0x10100000	0x101FFFFFFF	1 MB	PCIe root complex config space
0x10200000	0x103FFFFFFF	2 MB	HSM / security engine
0x10400000	0x10FFFFFFF	12 MB	Reserved
0x11000000	0x1FFFFFFF	240 MB	Fabric-attached device MMIO (GPU, NPU, etc.)
0x20000000	0x7FFFFFFF	1.5 GB	DRAM window 1 (general purpose)
0x80000000	0xFFFFFFFF	2 GB	DRAM window 2 (high mem / 64-bit alias)

3.2 64-bit Extension

For systems with >4 GB, the high address space is mapped via the MSR page table or MMU:

Table 4: BradXon high address space (48-bit)

Base	Size	Region
0x0000000000–0x00003FFFFFFF	256 GB	CPU-private DRAM
0x000040000000–0x00007FFFFFFF	256 GB	GPU-private DRAM
0x000080000000–0x0000FFFFFFFF	512 GB	SPMP shared (UVM)
0x000100000000–0x0001FFFFFFFF	512 GB	Infinity Buffer
0xFFFFF000000000–0xFFFF7FFFFFFF	512 GB	Fabric-attached I/O
0xFFFF8000000000–0xFFFFFFFFFFFF	512 GB	PCIe MMIO

4 Platform IP Blocks

4.1 XIC — BradXon Interrupt Controller

A central interrupt distributor modelled on ARM GIC-600 but simplified for the BradISA exception model.

Table 5: XIC register map (base: 0x10010000)

Offset	Name	Width	Description
0x0000	XIC_CTRL	32	Global enable, distributor routing
0x0004	XIC_STATUS	32	Pending interrupt bitmap
0x0008	XIC_CFG	32	Max IRQ lines, priority bits
0x0010	XIC_IRQ_ENABLE	32	Global IRQ enable mask
0x0014	XIC_IRQ_DISABLE	32	Atomic disable
0x0020	XIC_PRIO_THRESH	32	Priority threshold for taking IRQ
0x0100	XIC_SPI_BASE	32	Shared peripheral interrupt 0–31 config
0x0200	XIC_PPI_BASE	32	Private peripheral interrupt per core
0x0300	XIC_SOFT_IRQ	32	Software-generated interrupt
0x0400	XIC_TIMER_IRQ	32	Timer interrupt control

Interrupt lines:

- **SPI 0–15**: Platform devices (timer, UART, GPIO, WDT, DMA, I2C, SPI, RTC, PMU)
- **SPI 16–31**: Fabric-attached devices (GPU, NPU, HSM, HBM controller)
- **PPI 0–3**: Per-core private (timer, PMU alert, debug, WFI wake)
- **IRQ0–3**: Routed to BradISA exception vectors 0x20–0x2C

4.2 System Timer

Table 6: System timer register map (base: 0x10020000)

Offset	Name	Width	Description
0x0000	TIMER_FREQ	32	Timer frequency in Hz (fixed)
0x0004	TIMER_CNT_LO	32	Cycle counter low (free-running)
0x0008	TIMER_CNT_HI	32	Cycle counter high
0x0010	TIMER_CMP0	32	Compare value 0 (generates IRQ on match)
0x0014	TIMER_CMP1	32	Compare value 1
0x0018	TIMER_CMP2	32	Compare value 2
0x001C	TIMER_CMP3	32	Compare value 3
0x0020	TIMER_CTRL	32	Enable, reset, IRQ masks per comparator

4.3 UART — Debug Console

Table 7: UART register map (base: 0x10030000)

Offset	Name	Width	Description
0x0000	UART_DATA	8	Transmit / receive data
0x0004	UART_STATUS	8	TX ready, RX ready, error flags
0x0008	UART_CTRL	8	Enable, baud rate select, parity, stop bits
0x000C	UART_DIV	16	Baud rate divisor

Default: 115200 baud, 8N1, polling mode. FIFO depth: 16 bytes.

4.4 GPIO — General-Purpose I/O

Table 8: GPIO register map (base: 0x10040000)

Offset	Name	Width	Description
0x0000	GPIO_DATA	32	Pin values (read: input, write: output if configured)
0x0004	GPIO_DIR	32	Direction (0=input, 1=output)
0x0008	GPIO_PULL	32	Pull-up/pull-down enable
0x000C	GPIO_IRQ_EN	32	Interrupt on change enable
0x0010	GPIO_IRQ_STAT	32	Interrupt status (pending)

Supports up to 32 GPIO pins with configurable IRQ on rising/falling edge.

4.5 WDT — Watchdog Timer

Table 9: Watchdog register map (base: 0x10050000)

Offset	Name	Width	Description
0x0000	WDT_CTRL	8	Enable, reset enable, IRQ enable
0x0004	WDT_TIMEOUT	32	Timeout value in cycles
0x0008	WDT_RESTART	8	Write 0x5A to restart (pet)
0x000C	WDT_STATUS	8	Expired flag

On expiry: assert IRQ first; if not petted within second timeout, assert reset.

4.6 DMA — Direct Memory Access Controller

Table 10: DMA register map (base: 0x10060000)

Offset	Name	Width	Description
0x0000	DMA_CTRL	32	Global enable, priority, byte swap
0x0004	DMA_STATUS	32	Active channels bitmap
0x0010	DMA_CH_SRC	32	Channel 0 source address
0x0014	DMA_CH_DST	32	Channel 0 destination address
0x0018	DMA_CH_LEN	32	Channel 0 transfer length (bytes)
0x001C	DMA_CH_CTRL	32	Channel 0: start, inc src/dst, word size, IRQ enable
0x0020–0x003F			Channel 1–3 (same layout)

4 independent channels, each supporting memory-to-memory and memory-to-peripheral transfers. Word sizes: 8/16/32/64-bit. Supports linked-list descriptors for scatter-gather.

4.7 I2C Controller

Table 11: I2C register map (base: 0x10070000)

Offset	Name	Width	Description
0x0000	I2C_CTRL	8	Enable, master/slave, IRQ enable
0x0004	I2C_STATUS	8	Bus busy, ACK/NACK, arbitration lost
0x0008	I2C_ADDR	16	Target address (7 or 10 bit)
0x000C	I2C_DIV	16	Clock divider ($SCL = sys_clk / (div + 1) / 2$)
0x0010	I2C_DATA	8	Transmit / receive data byte
0x0014	I2C_CMD	8	Start, stop, read, write

4.8 SPI Controller

Table 12: SPI register map (base: 0x10080000)

Offset	Name	Width	Description
0x0000	SPI_CTRL	8	Enable, master/slave, CPOL, CPHA, loopback
0x0004	SPI_STATUS	8	Busy, TX empty, RX full
0x0008	SPI_DIV	16	Clock divider
0x000C	SPI_CS	8	Chip select (up to 4 devices)
0x0010	SPI_DATA	32	TX/RX data (up to 32-bit word)

4.9 RTC — Real-Time Clock

Table 13: RTC register map (base: 0x10090000)

Offset	Name	Width	Description
0x0000	RTC_TIME_SEC	32	Unix time (seconds since epoch)
0x0004	RTC_TIME_NSEC	32	Nanosecond fraction
0x0008	RTC_ALARM_SEC	32	Alarm seconds
0x000C	RTC_ALARM_CTRL	8	Alarm enable, IRQ enable
0x0010	RTC_BAT_STATUS	8	Battery voltage, low-battery flag
0x0020	RTC_BACKUP_SRAM	256	256-byte battery-backed SRAM

4.10 PMU — Power Management Unit

Table 14: PMU register map (base: 0x100A0000)

Offset	Name	Width	Description
0x0000	PMU_CTRL	32	Global enable, wake source select
0x0004	PMU_STATUS	32	Current C-state, P-state, voltage, frequency
0x0008	PMU_CSTATE	32	Request C-state transition
0x0010	PMU_PSTATE	32	Request P-state (voltage/freq pair index)
0x0014	PMU_VOLTAGE	32	Core voltage setpoint (mV)
0x0018	PMU_FREQ	32	Core frequency setpoint (MHz)
0x0020	PMU_TEMP	32	Die temperature ($^{\circ}\text{C} \times 100$)
0x0024	PMU_POWER	32	Instantaneous power draw (mW)
0x0028	PMU_ENERGY	64	Accumulated energy (μJ)
0x0030	PMU_PWR_CAP	32	Power cap (mW)
0x0034	PMU_TEMP_LIMIT	32	Thermal throttle temperature ($^{\circ}\text{C}$)
0x0038	PMU_TEMP_HALT	32	Thermal shutdown temperature ($^{\circ}\text{C}$)
0x0040	PMU_PWR_DOMAIN	32	Per-domain power gating control
0x0044	PMU_CLK_GATE	32	Per-unit clock gating mask
0x0050	PMU_FUSE	64	Fuse-embedded configuration

4.11 CRU — Clock and Reset Unit

Table 15: CRU register map (base: 0x100B0000)

Offset	Name	Width	Description
0x0000	CRU_PLL_CTRL	32	PLL configuration (N/M/D dividers, lock detect)
0x0004	CRU_PLL_STATUS	8	PLL lock status
0x0010	CRU_CLK_SEL	32	Clock source select per domain
0x0014	CRU_CLK_DIV	32	Clock divider per domain
0x0018	CRU_CLK_GATE	32	Clock gate enable per domain
0x0020	CRU_RESET_CTRL	32	Assert/de-assert reset per domain
0x0024	CRU_RESET_STAT	32	Reset status (in-reset flags)
0x0030	CRU_WDT_RESET	8	Watchdog reset status

Clock domains: CPU, Fabric, Memory, GPU, NPU, IO, AON (always-on).

5 Clock Architecture

Domain	Source	Max Frequency
CPU (P-core)	PLL0	5.2 GHz
CPU (E-core)	PLL0 (div)	2.4–3.6 GHz
Fabric (NoC)	PLL1	2.0 GHz
Memory (HBM)	PLL2	2.0 GHz (HBM3e @ 4.0 GT/s)
Memory (DDR)	PLL3	1.6 GHz (LPDDR6 @ 6.4 GT/s)
GPU	PLL4	2.5 GHz
NPU	PLL5	1.5 GHz
IO (PCIe)	PLL6	500 MHz (refclk)
Always-on	32 kHz RC + 32.768 kHz XTAL	32 kHz

Each PLL supports fractional-N synthesis with spread-spectrum modulation for EMI reduction. Clock gating at per-unit granularity via `CRU_CLK_GATE`.

5.1 Reset Domains

1. **POR** (Power-on reset): All logic resets. Released after PLL lock and voltage rail stabilisation.
2. **WARM** (System reset): CPU, GPU, NPU, peripherals reset. Memory and HBM content preserved.
3. **DEBUG** (JTAG reset): Debug logic only.
4. **WDT** (Watchdog reset): Same as WARM, triggered by watchdog expiry.

6 Boot Flow

1. **POR**: CRU holds all domains in reset. PMU waits for external power-good from board VRM.
2. **PLL lock**: CRU enables PLL0–PLL6, waits for lock detect.
3. **Boot ROM**: CPU 0 releases from reset, starts at 0x00000000. Boot ROM is mask-ROM at 0x00000000–0x0003FFFF.
4. **HSM attestation**: Boot ROM reads HSM status via sideband. HSM verifies boot ROM digest, releases measurement.
5. **Initialise platform**: Boot ROM configures CRU, PMU, XIC, UART. Prints banner at 115200 baud.
6. **Load Stage 2**: Boot ROM copies Stage 2 bootloader from SPI flash (or BradDrive) to SRAM at 0x00100000, verifies signature via HSM, then jumps to it.
7. **Stage 2**: Initialises DRAM controller (HBM + DDR), sets up page tables, loads kernel image, jumps to kernel entry.
8. **Kernel**: Initialises cores, fabric, devices, mounts rootfs, starts init.
Total cold boot time target: < 500 ms to kernel entry (Stage 2 loaded in < 100 ms from SPI flash).

7 Chiplet Topology

BradXon supports 1–4 identical compute chiplets (each on SF4X 4nm-class) connected via the BradFusion mesh fabric. Each chiplet contains:

- 4–8 Phoenix P-cores (BradXon configuration: 8-wide, 128-entry ROB)
- 0–8 Falcon/Kestrel E-cores
- 16–32 MB shared L3 cache per chiplet
- Local HBM3e controller (1–2 stacks, 128–256 GB/s each)
- Fabric router (2-D mesh, 4–8 directions)

7.1 Package Configurations

Table 16: BradXon chiplet configurations

SKU	Chiplets	P-cores	E-cores	L3 total	TDP
Xon 1P	1	4	4	32 MB	125 W
Xon 1E	1	8	8	48 MB	175 W
Xon 2P	2	12	8	80 MB	350 W
Xon 2E	2	16	16	96 MB	450 W
Xon 4P	4	24	16	160 MB	600 W
Xon 4X	4	32	32	192 MB	750 W

7.2 Fabric Routing

Each chiplet connects to its N/E/S/W neighbours via 8-lane differential links at 32 GT/s (256 GB/s per direction). A unified cache-coherent address space spans all chiplets using a directory-based MOESI protocol.

- On-chiplet latency: 2 ns per hop
- Cross-chiplet latency: 4 ns per chiplet boundary
- Max 4-chiplet diameter: 4 hops (chiplet 0 → chiplet 3)
- Total fabric bandwidth (4-die): > 2 TB/s bisection

8 Power Architecture

8.1 Voltage Rails

Table 17: BradXon power rail specifications

Rail	Min	Max	Max Current (Xon 4X)
VDD_CORE	0.55 V	0.90 V	500 A
VDD_FAB	0.70 V	0.85 V	50 A
VDD_MEM (HBM)	1.10 V	1.35 V	200 A
VDD_IO	1.80 V	1.80 V	20 A
VDD_PCIE	0.90 V	0.90 V	50 A
VDD_SEC	1.20 V	1.20 V	2 A (isolated)
VDD_STBY	5.00 V	5.00 V	1 A (always-on)

8.2 Power States

Table 18: BradXon platform power states

State	TDP	Description
P0	100%	Turbo — all cores max freq
P1	70%	Balanced — P-cores at 80% freq
P2	40%	Efficient — E-cores primary, P-cores gated
P3	10%	Retention — memory active, cores power-gated
P4	0.1%	Sleep — HBM self-refresh, wake on IRQ
P5	0.01%	Deep sleep — full power-down, RTC only

Transition latency: $P0 \leftrightarrow P1 < 1 \mu s$, $P0 \leftrightarrow P2 < 10 \mu s$, $P0 \leftrightarrow P3 < 100 \mu s$, $P0 \leftrightarrow P4 < 1 ms$, $P0 \leftrightarrow P5 < 50 ms$.

9 Peripherals and I/O

9.1 Integrated Peripherals

Table 19: BradXon peripheral inventory

Peripheral	Quantity	Notes
PCIe 6.0 root complex	1	1×16 or 2×8, 64 GT/s
USB4 v2 controller	1	80 Gbps, DP alt mode
10GbE MAC	1	RGMII/SGMII to external PHY
2.5GbE MAC	1	Integrated PHY
I2C controller	2	400 kHz / 1 MHz
SPI controller	2	Up to 50 MHz, 4 chip selects
UART	2	115200 baud debug + general purpose
GPIO	32	Multiplexed with alternate functions
PWM	4	16-bit resolution, fan control
I2S audio	1	Stereo, up to 192 kHz
SD Express 7.0	1	4 GB/s, SD card / eMMC

9.2 PCIe Root Complex

- Version: PCIe 6.0 (64 GT/s PAM-4)
- Lanes: 16 (configurable as 1×16, 2×8, 1×8+2×4)
- BAR space: 64-bit prefetchable
- ATS/SVM: Shared virtual memory with MMU
- Resizable BAR support for GPU

10 Security Architecture

Table 20: BradXon security layers

Layer	Engine	Coverage
L0	PUF (fabrication)	Die-unique key, never leaves hardware
L1	HSM (dedicated die)	Secure boot, attestation, key management
L2	SecBus (sideband)	Isolated bus for security-critical traffic
L3	AES-256-GCM (memory)	All DRAM encrypted at runtime
L4	AES-256-XTS (storage)	BradDrive transparent encryption
L5	Integrity (Merkle tree)	Tamper detection on all DRAM
L6	Zone isolation	Per-core VM isolation via MMU

10.1 HSM Specifications

- Process: 22 nm (cost-optimised, standalone die)
- Secure RAM: 512 KB (Nexus), 1 MB (Rack)
- Key slots: 128 (Nexus), 512 (Rack)
- Crypto engines: AES-256, SHA-3, RSA-4096, ECC, ML-KEM (PQC), ML-DSA
- Sideband: Dedicated I2C/SecBus to PMU, boot ROM, each chiplet

11 Revision History

Revision	Date	Changes
1.0	July 2026	Gen 1 re-tag; ANF section added (compute partitions, RDA, fabric governor + register map; Gen 2 vision note)
0.1	July 2026	Initial draft — memory map, IP blocks, boot flow, chiplet topology, power architecture, security