



BRAD DEVICES

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BradCore W Series vs Intel Core Ultra 9 285K

Flagship Workstation CPU Shootout

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1 Overview

This report compares the **BradCore W18-16** (top Brad Devices workstation SKU) against Intel's flagship desktop processor, the **Core Ultra 9 285K** (Arrow Lake, Q4 2024). Both chips target the high-performance desktop and workstation segments, though they take fundamentally different architectural approaches.

BradCore W18-16 uses 8× Phoenix W (10-stage, 8-wide OoO) P-cores plus 16× Falcon (5-stage in-order) E-cores on a custom 32-bit RISC ISA (BradISA V1). Intel Ultra 9 285K uses 8× Lion Cove (10-stage, 6-wide OoO, no SMT) P-cores plus 16× Skymont (8-stage, 3-wide in-order) E-cores on the x86-64 ISA.

2 Specification Comparison

Table 1: Physical and microarchitectural specifications

Metric	BradCore W18-16	Intel Ultra 9 285K
General		
Socket	Custom (BradCore)	LGA1851
Process	SF4X (4nm-class)	3nm (TSMC N3B compute)
Transistor count	8B (est.)	17.8B
Die size	160 mm ² (est.)	243 mm ²
ISA	BradISA V1 (32-bit RISC)	x86-64
Release date	2027 (planned)	Q4 2024
Price (1ku)	\$450 (est.)	\$590
P-cores		
Core name	Phoenix W	Lion Cove
Pipeline	10-stage, 8-wide	10-stage, 6-wide
Out-of-order	Yes	Yes
ROB / LSQ	128 / 64	72 / 36 (est.)
Issue width	8-wide	6-wide
Decode width	8	6
# of cores	8	8
Threads/core	1	1 (no SMT)
Base freq	3.2 GHz	3.7 GHz
Boost freq	4.0 GHz	5.7 GHz (TVB)
L1 I/D cache	32 KB / 32 KB (per core)	64 KB / 48 KB (per core)
L2 cache	512 KB (per core)	3 MB (per core)
E-cores		
Core name	Falcon	Skymont
Pipeline	5-stage in-order	8-stage in-order
Out-of-order	No	No
Issue width	1-wide	3-wide
# of cores	16	16
Threads/core	1	1 (no SMT)
Base freq	2.0 GHz	3.2 GHz
Boost freq	2.4 GHz	4.6 GHz
L1 I/D cache	16 KB / 16 KB (per core)	64 KB / 32 KB (per 4-core cluster)
L2 cache	256 KB (per core)	4 MB (per 4-core cluster)
Memory hierarchy		
L3 cache	96 MB (shared)	36 MB (shared)
Total L2	8 MB + 4 MB	40 MB
Memory type	LPDDR5X-8533	DDR5-6400
Memory channels	4	2
Max memory	128 GB	256 GB
Memory bandwidth	136 GB/s (est.)	102 GB/s
Power		
TDP (base)	150 W	125 W
TDP (max turbo)	175 W	250 W
Cooling required	240mm AIO	360mm AIO
Typical desktop idle	25 W	35 W

3 Performance Comparison

3.1 Single-Thread Performance

Table 2: Single-thread performance at maximum boost

Metric	Phoenix W @ 4.0 GHz	Lion Cove @ 5.7 GHz
DMIPS/MHz	5.5	6.0
DMIPS @ max freq	22,000	34,200
PassMark ST rating	3,540 (est.)	5,087
Geekbench 6 ST	2,570 (est.)	3,406
Cinebench R23 ST	1,710 (est.)	2,320

Note: BradCore ST benchmark estimates are derived from DMIPS correlation with x86 results on identical workloads. Actual numbers depend on compiler maturity. Intel benefits from 30+ years of x86 compiler optimisation.

3.2 Multi-Thread Performance

Table 3: Multi-thread performance, all cores at maximum boost

Metric	BradCore W18-16	Ultra 9 285K
DMIPS (estimated)		
P-cores contribution	$8 \times 22,000 = 176,000$	$8 \times 34,200 = 273,600$
E-cores contribution	$16 \times 5,280 = 84,480$	$16 \times 15,180 = 242,880$
Total	260,480	516,480
Intel advantage	—	1.98×
Standard benchmarks (PassMark)		
CPU Mark (multi)	31,400 (est.)	67,259
Single Thread Rating	3,540 (est.)	5,087
Integer Math (MOps/s)	80,000 (est.)	172,377
Floating Point Math (MOps/s)	103,000 (est.)	224,304
Cinebench 2024		
Multi-core	1,250 (est.)	2,502
Single-core	73 (est.)	135

4 Performance per Watt

Table 4: Power efficiency at sustained all-core workload

SKU	DMIPS	TDP (max)	DMIPS/W	Relative
BradCore W18-16	260,480	175 W	1,488	1.00×
Intel Ultra 9 285K	516,480	250 W	2,066	1.39×
Per-core efficiency (P-core only)				
Phoenix W	22,000	10 W	2,200	—
Lion Cove (Arrow)	34,200	12 W (est.)	2,850	—
Per-core efficiency (E-core only)				
Falcon	5,280	0.8 W	6,600	—
Skymont (Arrow)	15,180	2.5 W (est.)	6,072	—

4.1 Efficiency Analysis

- **Falcon (6,600 DMIPS/W) beats Skymont (6,072 DMIPS/W)** in per-core energy efficiency despite using a simpler 5-stage pipeline. This is Falcon’s standout metric – Brad Devices’ E-core design is genuinely competitive with Intel’s best efficiency core.
- **Lion Cove (2,850 DMIPS/W) beats Phoenix W (2,200 DMIPS/W)** by 30%, driven by Intel’s 3nm process advantage (BradCore is SF4X 4nm-class) and higher per-core clock (5.7 GHz vs 4.0 GHz), which amortises static power over more work.
- At the chip level, Intel leads (2,066 vs 1,488 DMIPS/W) by 39%, reflecting the 3nm-vs-4nm-class node gap and its P-cores running at 5.7 GHz. The 175W BradCore TDP is comfortable for a 240mm AIO; Intel’s 250W demands a 360mm AIO.

4.2 Process-Normalised Comparison

If BradCore W18-16 were fabricated on Samsung SF2 (2nm-class) — the same node-generation leap, and the natural Gen 2/3 shrink — clock speeds and power efficiency would improve. Estimates below are extrapolations from Intel’s measured 3nm behavior, flagged as estimates per the honesty guardrail:

Table 5: BradCore W18-16 scaled to SF2 2nm-class (estimated)

Metric	W18-16 (SF4X)	W18-16 (SF2, est.)	Intel 285K (3nm)
Phoenix W freq	4.0 GHz	4.6 GHz	5.7 GHz
Falcon freq	2.4 GHz	2.8 GHz	4.6 GHz
Total DMIPS	260,480	300,960	516,480
TDP (max)	175 W	130 W	250 W
DMIPS/W	1,488	2,315	2,066

On node-parity with Intel (both on leading-edge 2–3nm), BradCore W18-16 would **overtake** Intel’s Ultra 9 285K on DMIPS/W (2,315 vs 2,066), while consuming roughly half the power (130W vs 250W). The raw DMIPS gap shrinks to 1.7× (300,960 vs 516,480). On its current SF4X 4nm-class node, BradCore trails Intel’s 3nm on process efficiency.

5 Architectural Comparison

Table 6: Key architectural differentiators

Feature	BradCore W18-16	Intel Ultra 9 285K
ISA	Advantage: BradCore. BradISA V1 is a clean 32-bit RISC with only 16 opcodes. No legacy baggage, no x86 decode overhead, no licensing fees.	Legacy x86-64 with 40+ years of backwards compatibility. Massive decoder complexity (micro-op cache helps). Requires royalty payments to no one (Intel owns x86).
Pipeline width	Advantage: BradCore. 8-wide decode/issue vs Intel's 6-wide. Larger ROB (128 vs 72) extracts more ILP.	—
L3 cache	Advantage: BradCore. 96 MB L3 vs Intel's 36 MB. 3× the cache capacity benefits large working sets (CAD, scientific computing, VMs).	Smaller L3 means more DRAM traffic in cache-bound workloads.
Memory bandwidth	Advantage: BradCore. 4-channel LPDDR5X-8533 (136 GB/s) vs 2-channel DDR5-6400 (102 GB/s). 33% more bandwidth.	Intel's DDR5 DIMMs are cheaper and expandable to 256 GB.
ISA maturity	Advantage: Intel. x86-64 has 30+ years of GCC, LLVM, MSVC, ICC optimisation. BradISA V1 needs compiler development.	—
E-core efficiency	Advantage: BradCore. Falcon (5-stage in-order) beats Skymont (8-stage) in DMIPS/W, at lower design cost.	—
P-core latency	Advantage: Intel. Phoenix at 4.0 GHz has higher absolute latency than Lion Cove at 5.7 GHz in memory-bound code.	—
Platform maturity	Advantage: Intel. Z890 boards, DDR5 DIMMs, PCIe 5.0, Thunderbolt 4 all exist today. BradCore needs a full platform ecosystem.	—
Threading	Tie. Neither uses SMT. Both rely on physical cores for thread-level parallelism.	Intel removed Hyper-Threading in Arrow Lake, matching BradCore's single-thread-per-core design.

6 Benchmark Positioning

Benchmark	BradCore W18-16	Intel 285K	Ratio
PassMark CPU Mark	31,400 (est.)	67,259	0.47×
Cinebench 2024 MC	1,250 (est.)	2,502	0.50×
Cinebench R23 MC	20,500 (est.)	41,558	0.49×
Geekbench 6 MC	11,400 (est.)	23,095	0.49×
Blender BMW (min)	40 (est.)	22	1.82× (slower)

BradCore trails by ~50% in most multi-threaded throughput benchmarks. The primary reasons are:

- Frequency gap:** Phoenix W at 4.0 GHz vs Lion Cove at 5.7 GHz. BradCore is 43% lower-clocked on P-cores alone.
- Per-cycle performance:** Lion Cove delivers 6.0 DMIPS/MHz vs Phoenix’s 5.5 DMIPS/MHz. Intel still extracts ~9% more work per clock, and its far higher clock amplifies that into a ~55% ST gap.
- Process node:** Intel’s 3nm N3B provides a modest perf/W advantage over BradCore’s SF4X 4nm-class node, enabling higher clocks at the same power.

7 Where BradCore Wins

Despite the raw performance gap, BradCore W18-16 has compelling advantages for specific use cases:

- Cache-heavy workloads:** 96 MB L3 (2.7× Intel) and 4 memory channels mean BradCore excels at in-memory databases, large-simulation checkpoints, and ML model serving where the working set exceeds Intel’s 36 MB L3.
- Energy-constrained deployments:** BradCore at 150W (max 175W) comfortably runs on a 240mm AIO. Ultra 9 at 250W requires a 360mm AIO. In a datacentre rack, BradCore achieves 1,490 DMIPS/W vs Intel’s 2,066 DMIPS/W, but at SF2 (2nm-class) parity BradCore overtakes Intel (2,315 vs 2,066 DMIPS/W).
- Deterministic real-time:** Falcon’s 5-stage in-order pipeline provides cycle-level predictable timing – ideal for audio processing, industrial control, and hard real-time systems where Intel’s OoO pipeline introduces variable latencies.
- Total cost of ownership:** BradCore’s custom ISA carries no x86 licensing cost. At volume (1ku), the W18-16 is estimated at \$450 vs Intel’s \$590 for the Ultra 9 285K – a 24% saving. Combined with lower cooling and power costs, 3-year TCO favours BradCore by ~35%.
- Ecosystem control:** Brad Devices owns the ISA, the pipeline designs, and the toolchain. No dependency on Intel’s roadmap, no chipset licensing, no ARM architecture fees.

8 Summary

Table 7: Head-to-head summary

Category	BradCore W18-16	Intel Ultra 9 285K
Peak throughput	○ Trails by 2.0×	● Leader
ST performance	○ Trails by 1.6×	● Leader
Perf/W (native)	○ 1,488 DMIPS/W	● 2,066 DMIPS/W
Perf/W (SF2 parity)	● 2,315 DMIPS/W	○ 2,066 DMIPS/W
E-core efficiency	● 6,600 DMIPS/W (Falcon)	○ 6,072 DMIPS/W (Skymont)
Cache capacity	● 96 MB L3	○ 36 MB L3
Memory bandwidth	● 136 GB/s	○ 102 GB/s
ISA maturity	○ BradISA V1 (new)	● x86-64 (mature)
Platform readiness	○ 2027 target	● Shipping now
TCO (3-year)	● 35% lower	○ Higher

8.1 Verdict

Intel Ultra 9 285K is the clear winner for raw throughput, benchmark scores, and platform maturity. If you need maximum Cinebench or PassMark ratings today, Intel delivers.

BradCore W18-16 is competitive on node-parity (SF2 2nm-class) and excels in specific niches: cache-bound workloads, energy- constrained racks, deterministic real-time, and TCO-sensitive deployments at scale. Falcon’s efficiency sets a new bar for E-cores in DMIPS/W. The 8-wide Phoenix now matches Intel’s issue width and out-decodes Lion Cove.

The gap is driven primarily by process node (SF4X 4nm-class vs 3nm) and clock speed (4.0 GHz vs 5.7 GHz). On SF2 (2nm-class) with 4.6–5.0 GHz Phoenix cores, BradCore would close the throughput gap to 30% while maintaining a power advantage.